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CLAIMS

WHAT IS CLAIMED IS:

- 1 1. A memory system for converting virtual addresses into physical
2 addresses at the user code level and conveying the physical addresses to a
3 peripheral device, the system comprising:
4 a virtual memory having memory pages, each memory page
5 having a virtual memory address and a corresponding
6 physical memory address in a main memory;
7 a microprocessor having a translation look-aside buffer which
8 holds a subset of the virtual addresses for all the pages
9 and their corresponding physical memory addresses in the
10 main memory; and
11 a set of user-code level software instructions stored in said
12 main memory and executable by said microprocessor for
13 converting a virtual memory address into the
14 corresponding physical memory address, pinning the
15 page, and conveying the physical memory address to the
16 peripheral device at a user code level without requiring a
17 system call.
- 1 2. The memory system of claim 1, wherein the set of user-code
2 level software instructions directs the microprocessor to utilize the
3 translation look-aside buffer (TLB) in order to convert the virtual memory
4 address into its corresponding physical memory address and pin the page.
- 1 3. The memory system of claim 1, wherein the set of user-level
2 software instructions include instructions for unpinning the page, which

3 corresponds with the physical memory address conveyed to the peripheral
4 device, when the peripheral device has completed its operations.

1 4. The memory system of claim 1, further comprising a page pin
2 counter, which is incremented each additional time a page is pinned down
3 after a first time said page is pinned down.

1 5. The memory system of claim 1, wherein the set of user-level
2 software instructions include ²instructions for unpinning the page in memory,
3 by:

4 decrementing ⁶the page pin counter each time the page is to be
5 unpinned; and
6 unpinning ²the page which corresponds with the physical
7 memory address conveyed to the peripheral drive, once
8 the page pin counter has reached zero.

1 6. The memory system of claim 1, wherein the set of user level
2 software instructions include instructions for:

3 incrementing a per-process pin page counter each time a new
4 page is first pinned by ²the same process; and
5 incrementing a system wide pin page counter, each time a new
6 page is first pinned by any process within the system.

1 7. The memory system of claim 6 wherein the set of user level
2 instructions including instructions for:

3 checking the values in the per-process pin page counter and the
4 system wide pin page counter, each time a new page is
5 to be pinned within the system,

6 not pinning the new page associated with the physical address,
7 if either of these counters contains a value which
8 exceeds a maximum allowable value, otherwise pinning
9 the new page.

1 8. A method for converting a virtual address to a physical address
2 and conveying the physical addresses to a peripheral device at the user code
3 level, the method comprising:

4 executing user code and encountering an instruction which
5 requires the peripheral device to perform a memory
6 operation, the instruction containing a command which
7 describes the necessary operation, a virtual address of
8 the peripheral device which is to perform the memory
9 operation, and a virtual memory address which identifies
10 a page where the operation is to occur; and
11 executing a special user-code level instruction comprising the
12 further steps of:

13 translating the virtual memory address, where the
14 operation is to occur, into a physical memory
15 address location using a user code level
16 instruction set; and

17 transferring the command, which describes the
18 memory operation, and the physical memory
19 address location to the peripheral device via
20 a bus transaction, wherein the data portion
21 of the bus transaction will contain the
22 physical memory address location.

1 9. The method of claim 8, wherein the step of translating includes:
2 converting the virtual address which identifies a page where the
3 operation is to occur into a corresponding physical
4 memory address location using a translation look-aside
5 buffer resident in the microprocessor; and
6 pinning down the page which corresponds with the physical
7 memory address location.

1 10. The method of claim 9 wherein the translation look-aside buffer
2 has a number of entries, each entry containing a virtual address and a
3 corresponding physical address for a page.

1 11. The method of claim 9 wherein the step of pinning down the
2 page includes setting an extra bit space in a relevant entry in the translation
3 look-aside buffer which contains the physical memory address location which
4 is to be transferred to the peripheral device.

1 12. The method of claim 11, wherein a page pin counter is
2 incremented if the extra bit space in the relevant entry in the translation
3 look-aside buffer which contains the physical memory address location
4 transferred to the peripheral device has previously been set.

5 13. A method of claim 11 wherein the main memory contains a
6 page table which identifies all the pages in the main memory and their
7 corresponding virtual and physical memory addresses.

1 14. The method of claim 13, wherein the setting of the extra bit
2 space in the translation look-aside buffer, in order to pin the page, is

3 automatically written back into the page table so the page table also
4 indicates that the page has been pinned.

1 15. The method of claim 10 wherein the step of executing the
2 special user-code level instruction further includes:

3 unpinning the page, which corresponds with the physical
4 memory address conveyed to the peripheral drive, once
5 the peripheral device has completed its operations.

1 16. The method of claim 15, wherein the step of unpinning the
2 page includes:

3 decrementing a page pin counter which indicates a total
4 number of times the page to be unpinned has been
5 previously pinned;

6 clearing an extra bit space in a relevant entry in the translation
7 look-aside buffer which contains the virtual address of
8 the page to be unpinned, once the page pin counter has
9 reached zero.

1 17. The method of claim 8 wherein the step of executing the
2 special user-code level instruction further includes:

3
4 defining a physical address port space which can only be
5 written to by user-level code when using the special
6 instruction, the physical address port space holding the
7 physical address of the peripheral device that is to
8 perform the memory operation.

1 18. A set of user-code level software instructions executable by a
2 microprocessor for converting a virtual address to a physical address, pinning
3 an associated page, and conveying the physical address to a peripheral
4 device without requiring a system call, the instructions comprising:

5 a Trans_and_pin instruction for converting the virtual address to
6 a physical address, pinning the page associated with the
7 physical address and conveying the physical address to
8 the peripheral, the Trans_and_pin instruction including:

9 a <vaddr> source operand containing the virtual
10 address to be converted; and

11 a <target> source operand containing the address
12 of the peripheral device to which the
13 physical address is to be conveyed.

1 19. The set of user code level instructions of claim 18 wherein the
2 Trans_and_pin instruction increments a page pinned counter each time the
3 page associated with the physical address is pinned.

1 20. The set of user code level instructions of claim 18 wherein the
2 Trans_and_pin instruction:

3 increments a per-process pin page counter each time a new
4 page is first pinned by a process; and
5 increments a system wide pin page counter, each time a new
6 page is first pinned within the system.

1 21. The set of user code level instructions of claim 20 wherein the
2 Trans_and_pin instruction checks the per-process pin page counter and the
3 system wide pin page counter, each time a new page is first pinned within
4 the system, the Trans_and_Pin function not pinning the page associated with
5 the physical address, if either of these counters contains a value which
6 exceeds a maximum allowable value.

1 22. The set of user-code level instructions of claim 18 wherein the
2 Trans_and_pin instruction further includes:

3 an <outcome> destination operand containing information
4 which indicates whether the conversion of the virtual
5 address has been executed successfully or the reasons
6 for failure, if any.

1 23. The set of user-code level instructions of claim 18, further
2 comprising:

3 a Trans_and_pin_only instruction for converting the virtual
4 address to a physical address, pinning the page
5 associated with the physical address and storing the
6 physical address in a register location, the
7 Trans_and_pin_only instruction including:

8 a <vaddr> source operand containing the virtual
9 address to be converted; and
10 a <phy_addr_reg> destination operand containing
11 a register location where the physical
12 address is to be stored.

1 24. The set of user-code level instructions of claim 23 wherein the
2 register location specified in <phy_addr_reg> can only be written to in user-
3 level code by using the Trans_and_pin_only instruction.

1 25. The set of user-code level instructions of claim 24, wherein the
2 register location contains a valid bit which is set after the
3 Trans_and_pin_only instruction stores the physical address in the register
4 location.

1 26. The set of user code level instructions of claim 23 wherein the
2 Trans_and_pin_only instruction increments a page pinned counter each time
3 the page associated with the physical address is pinned.

1 27. The set of user-code level instructions of claim 23 wherein the
2 Trans_and_pin_only instruction further includes:
3 an <outcome> destination operand containing information
4 which indicates whether the conversion of the virtual
5 address to the physical address has been executed
6 successfully or the reasons for failure, if any.

1 28. The set of user-code level instructions of claim 23 and 25
2 further comprising:

3 a send_physical instruction for transferring the contents of the
4 register location specified in the Trans_and_pin_only
5 instruction to a peripheral device, the send_physical
6 instruction including:

7 a <phys_addr_reg> source operand which
8 specifies the register location; and

9 a <target> source operand containing the address
10 of the peripheral device.

1 29. The set of user code level instructions of claim 28 wherein the
2 send_physical instruction checks the valid bit in the register location
3 specified in <phys_addr_reg> to make sure it is set before transferring the
4 contents of the register location to the peripheral device.

1 30. The set of user code level instructions of claim 18 and 23,
2 further comprising:

3 an unpin instruction for unpinning the page previously pinned by
4 the Trans_and_pin or Trans_and_pin_only instruction once
5 the peripheral device is done using the page, the unpin
6 instruction including:

7 a <vaddr> source operand containing the virtual
8 address of the page to be unpinned.

1 31. The set of user code level instructions of claim 19 and 26
2 wherein the unpin instruction decrements the page pinned counter each time
3 the page is to be unpinned and then actually unpins the page only when the
4 contents of the page pin counter is zero.